

Kindly amend claims 1, 5, 6, and 7 as indicated below.

1. (Amended) A data capture system for latching an input data signal, comprising:

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a first data latch, coupled to receive an input data signal and a first data strobe signal, for generating a first latched data signal;

a second data latch, coupled to receive the input data signal and a second data strobe signal, for generating a second latched data signal;

a third data latch, coupled to receive the input data signal and a third data strobe signal, for generating a third latched data signal;

a first data comparator, coupled to receive the first latched data signal and the second latched data signal, for generating a delay more signal in response to the first latched data signal and the second latched data signal being not equal;

a second data comparator, coupled to receive the first latched data signal and the third latched data signal, for generating a delay less signal in response to the first latched data signal and the third latched data signal being not equal;

a delay controller, coupled to receive at least one of the delay more signal or the delay less signal, for generating an adjusting signal to adjust the delays of each data strobe signal[.];

a first delay element, coupled to receive a source data strobe signal and the adjusting signal from the delay controller, for generating the second data strobe signal;

a second delay element, coupled to receive the ^{second}~~first~~ data strobe signal and the adjusting signal from the delay controller, for generating the first data strobe signal; and

a third delay element, coupled to receive the ^{first}~~second~~ data strobe signal and the adjusting signal from the delay controller, for generating the third data strobe signal.

2. (Canceled).

3. The data capture system in claim 1, wherein the delay controller further comprises:

a threshold register for storing a threshold value;

a counter, coupled to receive the delay more signal or the delay less signal, for incrementing a counter value upon receiving the delay more signal or the delay less signal; and

a comparator, coupled to receive the threshold value and the counter value, for comparing the threshold value and the counter value and generating a qualified delay more or delay less signal in response to the counter value exceeding the threshold value.

4. The data capture system in claim 3, wherein the delay controller further comprises an OR latch for generating a software interrupt signal in response to receiving the qualified delay more signal or the qualified delay less signal.

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AG (Amended) The data capture system in claim [2] 1, wherein the delay controller further comprises an OR latch for generating a software interrupt signal in response to receiving the delay more signal or the delay less signal.

6. (Amended) In a data capture system, a method for ensuring capture of an input data signal, comprising:

receiving an input data signal at a first latch, a second latch, and a third latch;

receiving a first data strobe signal at the first latch, a second data strobe signal at the second latch, and a third data strobe signal at the third latch;

latching the input data signal at each latch in response to receiving the respective data strobe signal at that latch;

comparing the latched data from the first latch and the second latch to determine if the latched data is equal;

adjusting each data strobe signal individually to delay more in response to the latched data from the first latch and the second latch being not equal;

comparing the latched data from the second latch and the third latch to determine if the latched data is equal; and

adjusting each data strobe signal individually to delay less in response to the latched data from the second latch and the third latch being not equal.

7. (Amended) The method for ensuring capture of an input data signal in claim 6, wherein the adjusting each data strobe signal steps further comprise:

receiving the delay more signal or the delay less signal;

incrementing a counter value in response to receiving the delay more signal or the delay less signal;

comparing the counter value with a first threshold value in response to receiving a delay more signal and with a second threshold value in response to receiving a delay less signal;

generating a qualified delay more signal in response to the counter value incremented by the delay more signal exceeding the first threshold value; and

generating a qualified delay less signal in response to the counter value incremented by the delay less signal exceeding the second threshold value.

Kindly add new claim 8 as indicated below.

5. (New) The data capture system in claim 1, wherein the delay controller further comprises:

a delay matrix, coupled to receive the source data strobe signal, the delay matrix disposed to generate at least one delayed version of the source data strobe signal ;

a first delay selector circuit, coupled to receive the delay more signal and the delay less signal and coupled to the delay matrix;

a second delay selector circuit, coupled to receive the delay more signal and the delay less signal and coupled to the delay matrix; and

43 a third delay selector circuit, coupled to receive the delay more signal and the delay less signal and coupled to the delay matrix,

wherein each delay selector circuit is disposed to shift the source data strobe from the delay matrix in a first direction to increase delay in the adjustment signal in response to the input data signal drifting early and disposed to shift the source data strobe from the delay matrix in a second direction to decrease delay in the adjustment signal in response to the input data signal drifting late.

REMARKS

Claims 1-7 are pending in this application. Claims 1 and 5-7 are amended herein. Claim 2 is canceled. Applicant requests reconsideration and early allowance of claims 1 and 3-7. Applicant is submitting new claim 8, which Applicant believes to be patentably distinguishable over the cited references.

Claims 1-7 are rejected under 35 USC § 102(e) as being unpatentable over U.S. Patent Number 5,737,589 to Doi et al. ("Doi"). This rejection is now respectfully traversed.

Applicants have amended claim 1 to now recite a data capture system for latching an input data signal, wherein the system includes: